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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,913	01/09/2002	Rana P. Singh	SC11448TP P01	3167

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MOTOROLA INC
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EXAMINER	
GEBREMARIAM, SAMUEL A	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 01/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N . 10/045,913	Applicant(s) SINGH ET AL.	
	Examiner Samuel A Gebremariam	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

P riod f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,25-34 and 38-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,25-34 and 38-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Pri rity under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *10*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. In view of the appeal brief filed on 10/28/03, PROSECUTION IS HEREBY REOPENED. New grounds of rejections are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

The present application is reopened to clearly point out the position taken by the examiner in the previous office action. The office action below further explains why the reference of Shiozawa can be used for rejecting the method claims in the present application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-2, 5, 8-10,15, 19 and 23-27, 29 and 32-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Shiozawa et al., US patent No. 6,245,641.

Regarding claims 1 and 15, Shiozawa teaches (figs. 2-9) a method for forming a semiconductor device structure in a semiconductor layer, comprising: forming a first trench of a first width (4b, 4c) and a second trench of a second width (4a) in the semiconductor layer; forming a first insulator liner (5b, 5c and 8) in the first trench and a second insulator liner (5a and 8) in the second trench; forming a mask (11) over the second trench; etching at least a portion of the first insulator liner while the mask is over the second trench; removing the mask; and depositing an insulating layer (6) in the first trench and the second trench.

Shiozawa teaches more than one layer of oxide liner.

Regarding claim 2, Shiozawa teaches (fig. 3) the entire claimed process of claim 1 above including the first width (4b, 4c) is less than the second width (4a).

Regarding claim 5, Shiozawa teaches (figs. 4 and 5) the entire claimed process of claim 1 above including the step of forming the first insulator liner and the second insulator liner comprises growing oxide in the first trench and the second trench.

Regarding claim 8, Shiozawa teaches (fig. 8, col. 10, line 36-44) the entire claimed process of claim 1 above including the insulator layer comprises high-density plasma oxide fill.

Regarding claim 9, Shiozawa teaches (fig. 3) the entire claimed process of claim 1 above including forming a barrier layer (3a-3d) and a stress relief layer (2a-2d) over the semiconductor layer in areas adjacent to the first trench and the second trench.

Regarding claim 10, Shiozawa teaches (figs. 2 and 3) the entire claimed process of claim 1 above including a pad nitride (3a-3d) and pad oxide (2a-2d) over the semiconductor layer prior to forming the first trench and the second trench, and wherein the step of forming the first trench and the second trench comprises etching through selected portions of the pad nitride and the pad oxide and into the semiconductor layer.

Regarding claims 19 and 23-25, Shiozawa teaches (figs. 2, 3 and 7) the entire claimed process of claim 1 above including the step of forming the first insulator liner and the second insulator liner comprises growing oxide in the first trench and the second trench.

Regarding claims 26, 27 and 29, Shiozawa teaches (figs. 3, 7 and 8) the entire claimed process of claim 1 above including the step of forming the first insulator liner comprises growing oxide at a high temperature (figure 8 shows portion of the second insulator liner etched).

Shiozawa teaches forming thermal oxidation process for forming liners 5a to 5c (col. 9, line 14-30). This process inherently involves high temperature process.

Regarding claim 32, Shiozawa teaches the entire claimed process of claim 29 above including the first insulator liner (5b, 5c and 8) and the second insulator liner (5a and 8) comprises thermal oxide (col. 10, line 1-4).

Regarding claim 33, Shiozawa teaches the entire claimed process of claim 29 above including the step of depositing comprises filling the first trench and second trench (fig. 9).

Regarding claim 34, Shiozawa teaches (fig. 8, col. 10, line 36-44) the entire claimed process of claim 29 above including the insulating layer (6) comprises high-density plasma oxide (fig. 8).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3, 4, 6, 16, 17, 18, 22, 28, 40 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiozawa et al.

Regarding claim 3, Shiozawa teaches (fig. 7) the entire claimed process of claim 1 above except explicitly stating that the step of etching comprises completely removing the first insulator liner.

It is conventional in the art to completely remove oxide liners in a trench after forming them.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to completely remove the first liner oxide taught by Shiozawa since oxide liners are some times formed to minimize the damage done during etching process and removed afterwards.

Regarding claims 4, 22, 28, 40 and 42 Shiozawa teaches substantially the entire claimed process of claims 1, 15, 26 and 38 above except explicitly stating that the step

of etching results in leaving at least one hundred, fifty angstroms of the first and fifty angstroms of the second insulator liner.

Parameters such as thickness in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to vary the thickness of the oxide liner in the process of Shiozawa as claimed in order to form a trench isolation.

5. Claims 6, 16, 17, 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiozawa in view S. Wolf (Silicon Processing for The VLSI Era, volume 1, pages 532-533).

Regarding claims 6, 16, 17, 30, 31 Shiozawa teaches substantially the entire claimed process of claims 1,15 and 29 above except explicitly stating that the step of etching comprises a wet etch where the process comprises dipping the semiconductor device structure in hydrofluoric acid.

It is conventional and also taught by Shiozawa using wet etch process for removing portion of the oxide layer (8) in figure 12. Also hydrofluoric acid is a conventionally used etchant of oxide layer and is also taught by Wolf (starting paragraph 4 page 532).

It would have been obvious to one of ordinary skill in the art at the time the invention was made in corporate the conventional HF etchant Taught by Wolf in the process of Shiozawa because HF etches silicon oxide quickly for good process control.

6. Claims 7, 18, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiozawa in view of Lee US patent No. 5,994,201.

Regarding claims 7 and 18, Shiozawa teaches substantially the entire claimed process of claims 1 and 15 above except explicitly stating that the step of etching comprises applying etch chemistry to the semiconductor device.

The use of dry etching for removing oxide layer is a conventional process that is widely known and also taught by Lee (fig. 2E) for removing oxide layer (206).

It would have been obvious to one of ordinary skill in the art at the time the invention was made in corporate the conventional process of using dry etching process taught by Lee in the process of Shiozawa in order to uniformly etch the oxide liner.

Regarding claim 20, Shiozawa teaches substantially the entire claimed process of claims 1 and 15 above including the semiconductor layer has a top surface; the second trench has a corner where the trench adjoins the top surface of the semiconductor layer.

Shiozawa does not teach the step of forming the first insulator liner and the second insulator liner comprising rounding of the corner of the second.

Lee teaches (fig. 2c) forming liner (214) in such a way the corners in the trenches (210) and (212) are rounded.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include forming rounded corners as suggested by Lee in the process steps of Shiozawa in order to avoid kink effects that decrease the threshold voltage of the device (col. 2. line 9-20).

Regarding claim 21, Shiozawa teaches substantially the entire claimed process of claim 20 above including the corner is a semiconductor (fig. 2c).

7. Claims 38-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiozawa in view of Koike US patent No. 5,578,518.

Regarding claims 38-41, Shiozawa teaches substantially the entire claimed process of claims 20, 29, 32, 33 and 34 above including etching a portion of the second insulator liner (portion of 8a is removed figure 8).

Shiozawa does not teach growing a first insulator liner in the first trench and a second insulator liner in the second trench to achieve a radius of curvature of at least 200 Angstroms in the first and second corner.

Koike teaches (see abstract) rounding of isolation trenches to achieve a radius of curvature of not less than 500 angstroms. Furthermore parameters such as radius of curvature in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the radius of curvature of corners of the first and second trenches in the process of Shiozawa as taught by Koike since rounding of the edges prevents the concentration of electric field in the edge portion of the trench isolation resulting in the prevention of the lowering of the threshold voltage (col. 2, lines 43-47, Koike).

Response to Arguments

8. Applicant's arguments filed 10/28/03 have been fully considered but they are not persuasive. Applicant argues that growing an oxide layer is not the same as depositing an oxide layer. The examiner takes the position that growing an oxide layer is the same as depositing. Merriam-Webster's Collegiate Dictionary (2001), Tenth Edition, defines grow as "to increase in size by assimilation of material into the living organism or by accretion of material in a non-biological process". Since deposition process results in accretion of material, the two processes are the same. Therefore applicant's argument is rendered moot.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References A and B are cited as being related to trench isolation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel Admassu Gebremariam whose telephone number is 703 305 1913. The examiner can normally be reached on 8:00am-4: 30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 305-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Samuel Admassu Gebremariam
January 25, 2004

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